UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,307	08/19/2003	Louis L. Hsu	YOR920030075US1 (8728-613	8130

7590 03/27/2004

EXAMINER
VOCKRODT, JEFF B

ART UNIT	PAPER NUMBER
2822	

Frank Chau
F. CHAU & ASSOCIATES, LLP
Suite 501
1900 Hempstead Turnpike
East Meadow, NY 11554

DATE MAILED: 03/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,307	HSU ET AL.	
	Examiner	Art Unit	
	Jeff Vockrodt	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) *29-43* is/are withdrawn from consideration.

5)☒ Claim(s) *19-28* is/are allowed.

6)☒ Claim(s) *1-5 and 7-18* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/19/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the application papers filed on August 19, 2003.

Claims 1-45 are pending.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-28 and 44-45, drawn to a method of making a MIM capacitor, classified in class 438, subclass 250.

II. Claim 29-43, drawn to a MIM capacitor, classified in class 257, subclass 300.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the process of making (e.g. claim 1) requires a sequence of applying a mask and depositing a dielectric layer that is not necessary to make the product claimed (e.g. claim 29).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Michael Moreno on March 9, 2004 a provisional election was made with traverse to prosecute the invention of group I, claims 1-28 and 44-45. Affirmation of this election must be made by applicant in replying to this Office action. Claims 29-43 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 11-17 and 44 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,593,185 ("Tsai").

Tsai teaches a method of forming an embedded capacitor structure.

Claim 11. Tsai teaches forming a first metal layer ("prior metal line" 12); forming an insulating layer (16/18/20); forming a first via (26) and second via (24/22) (Fig. 3); depositing a mask (40, Fig. 5) over the second via (where contact 30) and portions of the insulating layer (16/18/20) ; etching through the mask down to the first metal layer (12) (see Fig. 5, left-most via); removing the mask (40) and forming a dielectric layer ("blanket insulator layer" 46, Fig. 6); depositing second metal layer (50, Fig. 7) and patterning the metal layer to remove a portion of the dielectric layer (46) (claim 11 does not require performing at least the last two steps in their written order).

Claim 12. The first and second vias include conductors (30, 32).

Claim 13. Layer 34 is a polish stop.

Claim 14. The dielectric (46) covers the entire substrate (Fig. 6).

Claim 15. Figs. 7-8 show patterning the second metal layer

Claim 16. Both metal layers can be copper (col. 5).

Claim 17. The mask 40 is photoresist.

Claim 44 is met by Fig. 3 of Tsai in which first vias (26) are for incorporation into a MIM capacitor and second via (22/24) is for incorporation into BEOL interconnects (compare w/ Fig. 10).

Claims 44-45 rejected under 35 U.S.C. 102(b) as being anticipated by U.S. 5,789,303 ("Leung").

Leung teaches a method of adding on chip capacitors to an integrated circuit.

Claim 44. Leung teaches simultaneously forming a via (220, Fig. 11) for a MIM capacitor and a via (222) for a BEOL interconnect (compare w/ Fig. 14).

Claim 45. Leung teaches simultaneously forming a BEOL interconnect (226) and a MIM capacitor (lower electrode 228).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5 and 7- 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,789,303 ("Leung") in view of US 2002/0155626 ("Park").

Claim 1. Leung teaches forming a first metal layer (204); forming a first insulating layer (214); forming a first opening (220) and a second opening (222); (forming a metal layer 228 over the first and second openings); patterning a dielectric layer (230) to leave dielectric over the metal layer 228 overlying the first opening (220); and depositing a first conductive material

(upper capacitor electrode 234) in the first and second openings. First, Leung does not teach the steps of depositing a mask over the second opening and removing the mask after depositing the dielectric layer. This sequence is known by those of ordinary skill in the art as a "lift-off" patterning procedure. Second, Leung does not teach "depositing a second metal layer over the first and second openings." This can be met by any additional metal layers such as a multi-layer upper electrode or further metallization layers.

Park teaches patterning a ferroelectric layer (26) using a lift-off process and forming an upper electrode (28) and barrier layer (29) over the ferroelectric layer. Park teaches that the lift-off process enables sputtering the ferroelectric layer, which is advantageous to spin-on techniques for improving uniformity. (¶¶ 6-7, 51.) Park teaches that the barrier layer improves control of contact resistance (¶ 0059).

Leung and Park are within the same field of endeavor -- on chip capacitors.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a "lift-off" process to pattern the dielectric 230 and to use a multilayer upper electrode in the process of forming the capacitor of Leung. One of ordinary skill in the art would have been motivated by the reasonable expectation that using a lift-off process would enable the use of sputtering for depositing the dielectric layer and thereby increase uniformity and by the reasonable expectation that the use of a barrier layer would control contact resistance.

Claim 2. Layer 216 of Leung is capable of serving as a polish stop (see other embodiment Figs. 6-7).

Claim 3. Fig. 11 of Leung shows etching down to the metal layer (204).

Claim 5. The metal layer 254 is over both first and second openings.

Claims 7 and 9. Tungsten and copper are explicitly taught (col. 11, ll. 60-67).

Claim 8. The mask is a photoresist (Park, ¶ 43).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Leung and Park as applied to claims 1-5 and 7-9 above, and further in view of US 5,926,359 ("Greco").

Leung is discussed above and teaches that silicon dioxide can be used as a dielectric material (col. 11, ll. 30-35), Leung prefers higher dielectric constant materials. Nevertheless, Leung teaches that silicon dioxide can be used. Leung does not teach CVD of silicon dioxide.

Greco shows that CVD of TEOS is a preferred method of depositing silicon dioxide for use as a capacitor dielectric. (col. 3, ll. 50-60.)

It would have been obvious to one of ordinary skill in the art at the time of the invention to deposit the silicon dioxide dielectric of Leung using CVD as described by Greco. One of ordinary skill in the art would have been motivated to use CVD as it was known method for the purpose of forming a dielectric layer for a capacitor as shown by Greco.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai in view of Park.

Tsai is applied to claims 11-17 and 44 above. Tsai teaches that its dielectric can be silicon oxide or silicon nitride (col. 5, ll. 25-30), but does not teach using CVD.

Greco shows that CVD of TEOS is a preferred method of depositing silicon dioxide for use as a capacitor dielectric. (col. 3, ll. 50-60.)

It would have been obvious to one of ordinary skill in the art at the time of the invention to deposit the silicon dioxide dielectric of Tsai using CVD as described by Greco. One of ordinary skill in the art would have been motivated to use CVD as it was known method for the purpose of forming a dielectric layer for a capacitor as shown by Greco.

Allowable Subject Matter

Claims 19-28 allowed.

Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The closest reference to claim 19 (from which claims 20-28 depend) is US 2002/0028552 ("Lee"). Lee teaches forming a spacer (208) in a capacitor region and meets many of the other method limitations of claim 19, but does not teach removing a predetermined portion of the sidewall liner material to form spacers on each sidewall of the second opening (the opening in which the dielectric layer is removed from subsequently, i.e., the contact opening as opposed to the capacitor opening). Thus, Lee does not teach or suggest the invention of claim 19.

Claim 6 is objected to because Leung does not teach or suggest forming additional capacitors in subsequent metallization layers as would be required to meet all of the limitations of claim 6.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,426,250 and US 6,025,226 teach other interconnect capactior configurations.

Any inquiry concerning communications from the examiner should be directed to Jeff Vockrodt at (571) 272-1848. The examiner can be reached on weekdays from 9:30 am to 5:00 pm EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian, can be reached at (571) 272-1852.

The fax number for official correspondence is (703) 872-9306. Unofficial communications to the examiner may be faxed to (571) 273-1848. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist at (703) 308-0956.

March 11, 2004
J. Vockrodt

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800